[0012] United States Patent No. 6,044,015, issued on March 28, 2000, entitled "Method of programming a flash eeprom memory cell array optimized for low power consumption";

[0013] United States Patent No. 6,366,500 B1, issued on April 2, 2002, entitled "Process for making and programming and operating dual-bit multi-level ballistic flash memory"; and

[0014] United States Patent No. 6,580,120, issued on June 17, 2003, entitled "A non-volatile electrically alterable semiconductor memory device and methods of operating such device"; and

[0015] This application hereby incorporates by reference the following U.S. Patent Applications in their entirety:

[0016] United States Provisional Patent Application No. 60/161,275, filed October 25, 1999, entitled "A non-volatile electrically alterable semiconductor memory device and methods of operating such device";

[0017] United States Provisional Patent Application No. 60/296,618, filed June 8, 2001, entitled "Two bit non-volatile electrically erasable and programmable memory structure, a process for producing said memory structure and methods for programming and erasing said memory structure"; and

[0018] United States Application No. 10/156,421, filed May 28, 2002, entitled "Memory system for multibit storage and method for storing and reading out data in said system".

[0019] This application hereby incorporates by reference the following European Patent Applications in their entirety:

[0020] European Patent Application No. EP008701458, filed October 25, 2000, entitled "A non-volatile electrically alterable semiconductor memory device and methods of operating such device";

[0021] European Patent Application No. 00870245.8, filed October 25, 2000 entitled "Electrically programmable and erasable memory device and method of operating the same", which published as European Publication No. 1096572 A1 on May 2, 2001.